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Novel Three Phase Five Level Inverter with Reduced Number of Power Electronics Components

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Abstract: *Novel three phase five level inverter with reduced number of power electronics components are introduced. This inverter consists of typical three phase two level-bridge inverter with three bidirectional switches and two cascaded h bridge is added into the inverter. Fundamental frequency Staircase modulation technique is used to giving the switching gate signals to the novel three phase five level inverter. Novel three phase five level inverter is compared with conventional three phase five level inverter topologies. Simulation and results of proposed inverter is given.*

Keywords- *Bidirectional switches,cascaded h bridge inverter, fundamental frequency staircase modulation, multilevel inverter,three phase two level bridge inverter.*

I. Introduction

Multilevel inverter (MLI) is a power electronics device which is mostly used in many industrial applications now a days. MLI has capable of providing desired AC voltage level at the output, using many lower level DC voltages as an input. MLI is mainly classified into three types. They are (1) Neutral Point clamped inverter (NPC), 2).Flying Capacitor inverter (FC),(3).Cascaded H-Bridge inverter(CHB). Different types of MLI circuit topologies and populous collection of control strategies are summarized in the literature[1]-[3].The main drawbacks of above topologies are, capacitor voltage balancing in the NPC, the output which is produced by FC is half of its input voltage, and large amount of separate dc supplies in CHB which are elaborated in the literature[4],[5].Aside from these three main topologies, alternative topologies like Multilevel DC link inverter are described in the literature[6]-[17].In recent times, the research area gives importance to hybrid multilevel and asymmetrical multilevel inverter topologies. The price and size of these topologies are diminished. And improve the accuracy seeing that fewer number of dc supplies, capacitors, switches and power electronics elements are used. Unequal dc supplies are used in hybrid multilevel inverters and this inverter consists of various multilevel configurations. Distinct Modulation techniques and power electronics components are required with this type of converter [18]-[19].Various topologies and distinct types of bidirectional switches were recommended for the purpose of improving the performance of typical single phase and three phase inverters [20]-[22].Contrast to unidirectional switch, bidirectional switch has ability to hold off the voltage and conduct the current in both direction. The proper control strategies are used in bidirectional switches in order to increase the performance of MLI in terms of compressing the total count of semiconductor devices, reducing the hold off voltage and producing the desired higher level output voltage[22]-[24].Depend on this technology ,this manuscript recommended a new topology for three phase five level inverter. Less number of power electronics components and insulated gate drive circuits are used in this inverter. Price and installation area are also decidedly minimized. By selecting appropriate degrees of utilized dc supplies we can obtain the required higher level voltage with adequate operation of fundamental frequency staircase modulation technique.

II. Operation of novel topology

Fig.(1) and (2) shows a classic configuration of three phase five level inverter which consists of typical three phase two level bridge inverter(Q1-Q6) .Three bidirectional switches (S1-S6, Dr1-Db2) two switches and two diode types are added with typical three phase two level bridge inverter. The operation of bidirectional switches is to hold off the higher voltage and ease the current flow to and from the midpoint (o).The fixed $4V_{dc}$ supply is given to the multilevel dc link inverter. Here two cascaded H-bridge (CHB) cells are used. These two CHB cells are having two unequal DC supplies .First cell has supply voltage of V_{dc} and Second cell has supply voltage of 2Vdc which are connected in (+, 0,-) bridge terminals.

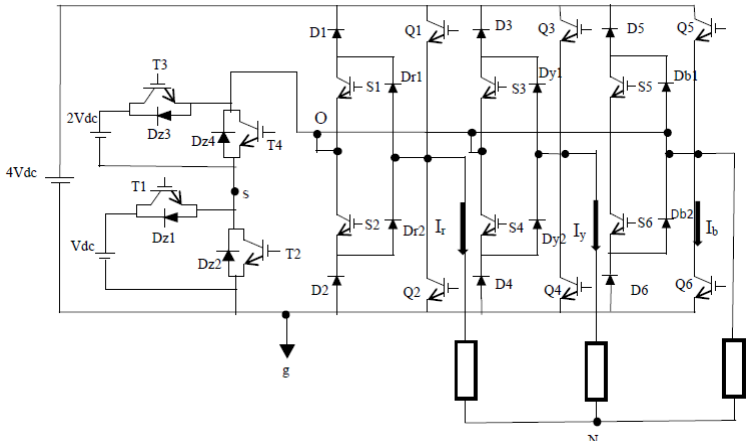

Fig.1 configuration of novel three phase five level inverter.

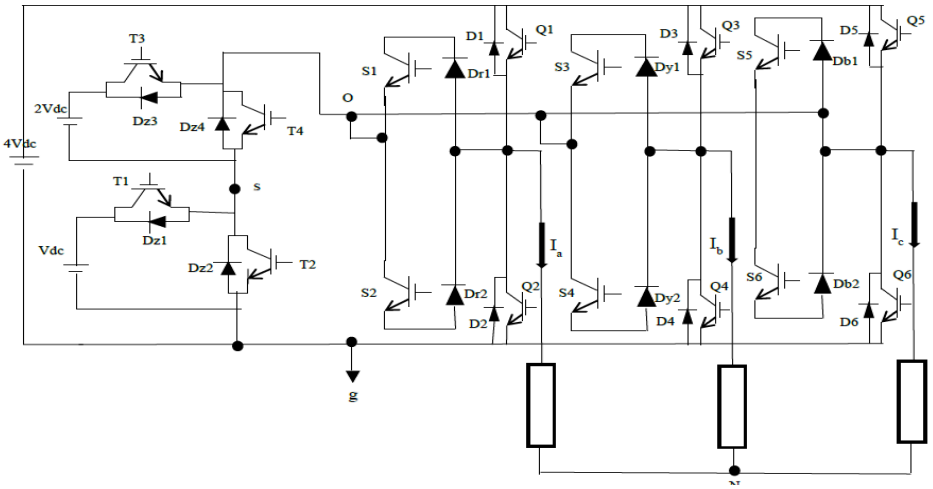

Fig.2 configuration of novel three phase five level inverter.

Depend on required voltage level, the total count of CHB cells are used. In this manuscript, the suggested inverter construct to produce a five level output voltage, hence here two CHB cells are used in series with two unequal dc supplies. The two switches from the each cell is turned ON and OFF under inverted condition. When T1 is turned ON the V_{dc} of first cell supply is added $V_{sg}=+V_{dc}$ where V_{sg} is the voltage at the node(s) with respect to ground (g), if T2 is turned ON $V_{sg}=0$.In the same way, When T3 is turned ON the 2Vdc of second cell supply is added $V_{os}=+2V_{dc}$ where V_{os} is the voltage at midpoint(0) with respect to node(m).4Vdc is the peak voltage rating of typical three phase two level bridge inverter(Q1-Q6) While 3Vdc is the peak voltage rating of three bidirectional switches(S1-S6). The first cell of CHB (T1, T2) has the peak voltage rating of V_{dc} and the second cell of CHB (T3, T4) has the peak voltage rating of 2Vdc. From phase r the conducting status of the switches and inverter line to ground V_{rg} are given in Table 1.

Table 1. Switching state S_r and inverter line to ground voltage V_{rg}

S_r	Q1	S1	S2	Q2	T1	T2	T3	T4	V_{rg}
4	on	off	off	off	on	off	on	off	+4Vdc
3	off	on	on	off	on	off	on	off	+3Vdc
2	off	on	on	off	off	on	on	off	+2Vdc
1	off	on	on	off	on	off	off	on	+Vdc
0	off	off	off	on	on	off	off	on	0

It is easier to define the inverter line-to-ground voltages V_{rg} ,V_{yg} , and V_{bg} in terms of switching states S_r, S_y, and S_b as,

$$\begin{bmatrix} Vrg \\ Vyg \\ Vbg \end{bmatrix} = \frac{4Vdc}{M-1} * \begin{bmatrix} Sr \\ Sy \\ Sb \end{bmatrix} (1)$$

Where M is the maximum number of voltage levels.

The switching state sequences of the suggested inverter is given in table II. The required balanced output voltages will be produced if the suggested inverter operates on the switching states which are given in the table 2. The proposed inverter have twenty four distinct modes with in a one cycle of output waveform .As stated in Table II, we know that the bidirectional switches are conduct only in eighteen modes. In all modes, there is only one bidirectional switch is in ON state.From this we can observe that the load current can be commutates through one switch and one diode. (For instance: in (410), the load current I_y can flow in S3 and Dy1 or S4 and Dy2).Seeing that, few insulated bipolar transistors (IGBTs) share the similar switching gate signals, the suggested configuration decidedly granted in minimizing the switching devices and complexity of the system.

Table 2.Switching state sequence of the novel topology within one cycle

Sr Sy Sb	Period[Ts]	ON Switches Leg r	ON Switches Leg y	ON Switches Leg b	ON Switches cascaded half-bridge	Vrg	Vyg	Vbg
400	t1	Q1	Q4	Q6	T1,T4	4Vdc	0	0
410	t2	Q1	S3,S4	Q6	T1,T4	4Vdc	Vdc	0
420	t3	Q1	S3,S4	Q6	T2,T3	4Vdc	2Vdc	0
430	t4	Q1	S3,S4	Q6	T1,T3	4Vdc	3Vdc	0
440	t5	Q1	Q3	Q6	T1,T3	4Vdc	4Vdc	0
340	t6	S1,S2	Q3	Q6	T1,T3	3Vdc	4Vdc	0
240	t7	S1,S2	Q3	Q6	T2,T3	2Vdc	4Vdc	0
140	t8	S1,S2	Q3	Q6	T1,T4	Vdc	4Vdc	0
040	t9	Q2	Q3	Q6	T1,T4	0	4Vdc	0
041	t10	Q2	Q3	S5,S6	T1,T4	0	4Vdc	Vdc
042	t11	Q2	Q3	S5,S6	T2,T3	0	4Vdc	2Vdc
043	t12	Q2	Q3	S5,S6	T1,T3	0	4Vdc	3Vdc
044	t13	Q2	Q3	Q5	T1,T3	0	4Vdc	4Vdc
034	t14	Q2	S3,S4	Q5	T1,T3	0	3Vdc	4Vdc
024	t15	Q2	S3,S4	Q5	T2,T3	0	2Vdc	4Vdc
014	t16	Q2	S3,S4	Q5	T1,T4	0	Vdc	4Vdc
004	t17	Q2	Q4	Q5	T1,T4	0	0	4Vdc
104	t18	S1,S2	Q4	Q5	T1,T4	Vdc	0	4Vdc
204	t19	S1,S2	Q4	Q5	T2,T3	2Vdc	0	4Vdc
304	t20	S1,S2	Q4	Q5	T1,T3	3Vdc	0	4Vdc
404	t21	Q1	Q4	Q5	T1,T3	4Vdc	0	4Vdc
403	t22	Q1	Q4	S5,S6	T1,T3	4Vdc	0	3Vdc
402	t23	Q1	Q4	S5,S6	T2,T3	4Vdc	0	2Vdc
401	t24	Q1	Q4	S5,S6	T1,T4	4Vdc	0	Vdc

The inverter line-to-line voltage V_{ry}, V_{yb}, V_{br} are related to V_{rg},V_{yg},and V_{bg} by

$$\begin{bmatrix} Vry \\ Vyb \\ Vbr \end{bmatrix} = \begin{bmatrix} 1 & -1 & 0 \\ 0 & 1 & -1 \\ -1 & 0 & 1 \end{bmatrix} * \begin{bmatrix} Vrg \\ Vyg \\ Vbg \end{bmatrix} \quad (2)$$

The inverter line-to-neutral voltages V_{rN},V_{yN}, and V_{bN} may be expressed

$$\begin{bmatrix} VrN \\ VyN \\ VbN \end{bmatrix} = \frac{1}{3}\begin{bmatrix} 2 & -1 & -1 \\ -1 & 2 & -1 \\ -1 & -1 & 2 \end{bmatrix} * \begin{bmatrix} Vrg \\ Vyg \\ Vbg \end{bmatrix} \quad (3)$$

It is helpful to observe that the inverter voltages at terminals r, y, and b with respect to the midpoint (o) are given by

$$\begin{bmatrix} Vro \\ Vyo \\ Vbo \end{bmatrix} = \begin{bmatrix} Vrg \\ Vyg \\ Vbg \end{bmatrix} - \begin{bmatrix} Vog \\ Vog \\ Vog \end{bmatrix} \quad (4)$$

Where V_{og} is the voltage at the midpoint(o) with respect to ground(g).V_{og} normally oscillate between three distinct voltage values Vdc,2Vdc,and 3Vdc as follows:

$$V_{og}=\begin{cases} Vdc, & If\ Sr+Sy-Sb \le 5. \\ 2Vdc, & if\ Sr+Sy-Sb = 6. \\ 3Vdc, & if\ Sr+Sy-Sb \ge 7. \end{cases} \quad (5)$$

For example, 13 sequent voltage steps are seen in V_{rN} waveform as follows: +8Vdc /3, +7Vdc /3, +6Vdc /3, +5Vdc /3, +4Vdc /3, +2Vdc /3, 0, –2Vdc /3, −4Vdc /3, –5Vdc /3, –6V dc/3, −7Vdc /3, and –8Vdc /3. From this we notice that all simulated output waveforms are attained at t1=t2 = ⋯ = t24 = 0.02/24s.

III. DQ Transformation

Clarke and Park transformations are used in high performance architectures in three phase power system analysis. Current and voltage are represented in terms of spacevector which is represented in a stationary reference frame. A general rotating reference frame has then been introduced. This frame is described by d and q axes .Clarke, Park and Inverse Park transformations have been described. Through the use of the Clarke transformation, the real and imaginary currents can be identified. The Park transformation is used to realize the transformation of those real and imaginary currents from the stationary to the rotating reference frame.

Fig.3 Block diagram of Clarke and Park transformation

3.1 d-q Rotating Reference Frame

Let us now convert x and y axes into d and q axes. Assume ψbe a vector along d-axis as shown in Fig. 6.3

In (α, β) plane,

$$\psi = \psi\alpha + \psi\beta \quad (6)$$

In (d, q) plane,

$$\psi = \psi_d + \psi_q \quad (7)$$

Angle between (α, β*) and (*d, q*) is* θ. Then

$$\sin\theta = \frac{\psi\beta}{\psi d} \quad (8)$$

$$\cos\theta = \frac{\psi\alpha}{\psi d} \quad (9)$$

The following transformations are involved due to rotation of orthogonal d-q system

1. α-βto d-q: Park transformation
2. d-q to α-β: Inverse Park transformation

Transformation from (*α*, β) to (*d*, *q*) is done by

$$\begin{bmatrix} d \\ q \end{bmatrix} = \begin{bmatrix} \cos\theta & \sin\theta \\ -\sin\theta & \cos\theta \end{bmatrix} * \begin{bmatrix} \alpha \\ \beta \end{bmatrix} \quad (10)$$

(or)

$$\begin{bmatrix} d \\ q \end{bmatrix} = [\text{Park Matrix}] * \begin{bmatrix} \alpha \\ \beta \end{bmatrix} \quad (11)$$

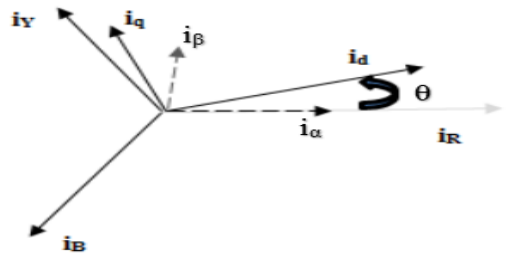

Fig.4 R-Y-B, (α, β) and (d, q) current reference frames.

Voltages in Clarke plane can be obtained from phase voltages as follows

$$\begin{bmatrix} V\alpha \\ V\beta \end{bmatrix} = [Clarke\ Matrix] * \begin{bmatrix} VR \\ VY \\ VB \end{bmatrix} \quad (12)$$

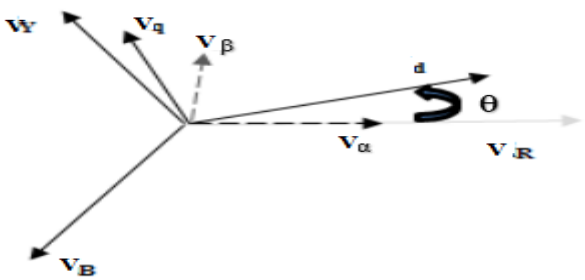

Fig.5 R-Y-B, (α, β) and (d, q) Voltage reference frames

Voltages in Park plane can be obtained from Clarke plane voltages as follows

$$\begin{bmatrix} Vd \\ Vq \end{bmatrix} = [Park\ Matrix] * \begin{bmatrix} V\alpha \\ V\beta \end{bmatrix} \quad (13)$$

3.2 Space vector diagram for the proposed topology:

The below equations are used to derive the d and q voltage vectors to plot the space vector diagram of the new three phase inverter which is suggested in this manuscript.

$V_q = \frac{4Vdc}{3(N-1)}(2S_a - S_b - S_c)$ (14)

$V_d = \frac{4Vdc}{\sqrt{3}(N-1)}(S_c - S_b)$ (15)

$V = V_q - jV_d$. (16)

Switching states which are given in table 2, Fig. 6 shows the space vector diagram for the proposed topology

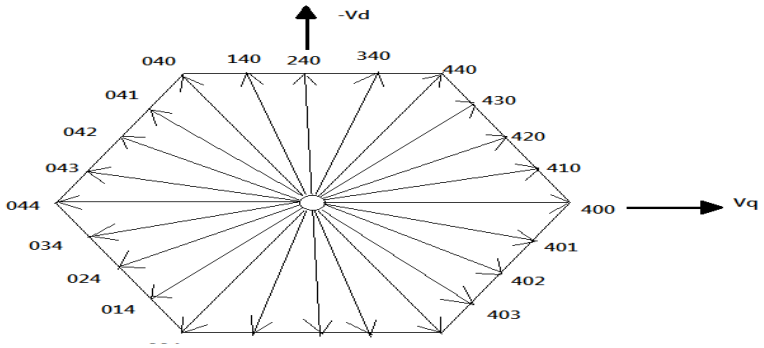

Fig.6 Space vector diagram for the proposed topology

IV. Switching algorithm

To remove the unwanted harmonic components and to control the fundamental voltage, the Staircase modulation with selective harmonic elimination technique is used in the proposed topology .Newton-Rapson method is an iterative method which is used to solve the non-linear (M-1) equations. But the calculation of this method is very difficult and it takes more time to compute. This method needs a high performance controllers for real time applications these are the main drawbacks of this method. Hence the other method is used to produce appropriate switching gate signals of the proposed inverter. This method is used to control the new three phase proposed inverter. By using this method, the desired output voltage waveforms can be produced in terms of S_r, S_y, and S_b. The fundamental of the Staircase modulation technique can be described as following: The operation of the proposed inverter, within the full cycle of the inverter the switching states S_r, S_y, and S_b are decided immediately for a selected value of modulation index Ma. The on-time calculations of S_r, S_y, and S_b directly based on the immediate values of the inverter line-to-ground voltages. It is well known as the reference values of V_{rg} ,V_{yg} , and V_{bg} are given b

$$\begin{bmatrix} Vrg_{\_ref} \\ Vyg_{\_ref} \\ Vbg\_ref \end{bmatrix} = \frac{Ma*4Vdc}{2} * \begin{bmatrix} \cos(wt) \\ \cos(wt - \frac{2}{3}) \\ \cos(wt + \frac{2}{3}) \end{bmatrix} + \frac{4Vdc}{2} * \begin{bmatrix} 1 \\ 1 \\ 1 \end{bmatrix} \quad (17)$$

$$\begin{bmatrix} Vrg_{\_ref} \\ Vyg_{\_ref} \\ Vbg\_ref \end{bmatrix} = \frac{Ma*4Vdc}{2} * \begin{bmatrix} \cos(wt) \\ \cos(wt - \frac{2}{3}) \\ \cos(wt + \frac{2}{3}) \end{bmatrix} + \frac{4Vdc}{2}$$

$$\begin{bmatrix} Sr \\ Sy \\ Sb \end{bmatrix} = \left(\frac{M-1}{4Vdc} * \begin{bmatrix} Vrg_{\_ref} \\ Vyg_{\_ref} \\ Vbg\_ref \end{bmatrix} \right). \quad (19)$$

Contrast to staircase modulation with selective harmonic method, the proposed modulation method requires fewer time and needs only easy calculations .The inverter's operating switching states S_r, S_y, and S_b and appropriate switching gate signals depend on the proposed modulation method. From this we know that the switching gate signals are produced within twenty four distinct modes starting from (044) to (034).

V. Comparison study

To test the performance of suggested configuration, the novel topology is compared with the typical multilevel three phase five level inverter topologies such as FC, CHB and NPC. It is proved that the novel three phase five level inverter requires less number of power electronics components when compared with conventional topologies with same number of voltage stages. For the five level output voltages the Table 3 explains the required number of dc voltage supplies, switches, clamping diodes,control signals and balancing capacitors of the novel three phase M level inverter compared with conventionalinverters such as CHB,Fc and NPC,and Table 4 explains the required voltage rating of conventional and proposed topology.

Table 3. Comparison of three phase five level conventional topologies with novel three phase five level inverter

Converter type	NPC	FC	CHB	Proposed inverter
Switches	6(M-1)	6(M-1)	6(M-1)	$\sqrt{8M-15}+11$
Gate drives	6(M-1)	6(M-1)	6(M-1)	$\sqrt{8M-15}+8$
Diodes	6(M-1)	6(M-1)	6(M-1)	$\sqrt{8M-15}+11$
Clamping diodes	6(M-2)	0	0	0
Dc supplies	M-1	M-1	3(M-1)/2	$1+[\sqrt{8M-15}-1/2]$
Clamping capacitors	0	3(M-1)	0	0
Control signals	6(M-1)	6(M-1)	6(M-1)	$\sqrt{8M-15}+8$

Table 4.Proposed and the existing topologies rating requirements per level N

Novel three phase five level inverter	Main bridge Q1-Q6 Da1-Dc2	Bidirectional switches S1 to S6 D1 to D6	Cascaded Half-Bridge switches T1 to T4		Converter type	NPC	FC	CHB
			1^{st}cell	2^{nd} cell	Switches Voltage rating	V_{dc}	V_{dc}	V_{dc}
Component voltage rating	$(N-1)V_{dc}$	$(N-2)V_{dc}$	V_{dc}	$2V_{dc}$	Clamping diode voltage rating	V_{dc}	0	0
					Clamping capacitor voltage rating	0	V_{dc}	0

VI. Simulation and Results

To ensure the workability of the proposed topology, the inverter was executed. The inverter which isshown in Fig. 1 and Fig.2 was investigated under V_{dc}= 22.5 V in the first cell, $2V_{dc}$=45V in the second cell and $4V_{dc}$= 90V. The degree of the fixed dc supply is determined as V_{fix}=$4V_{dc}$=90V. Fixed three-phase series resistive–inductive load (23Ω–3 mH/Phase) in star connection was used.

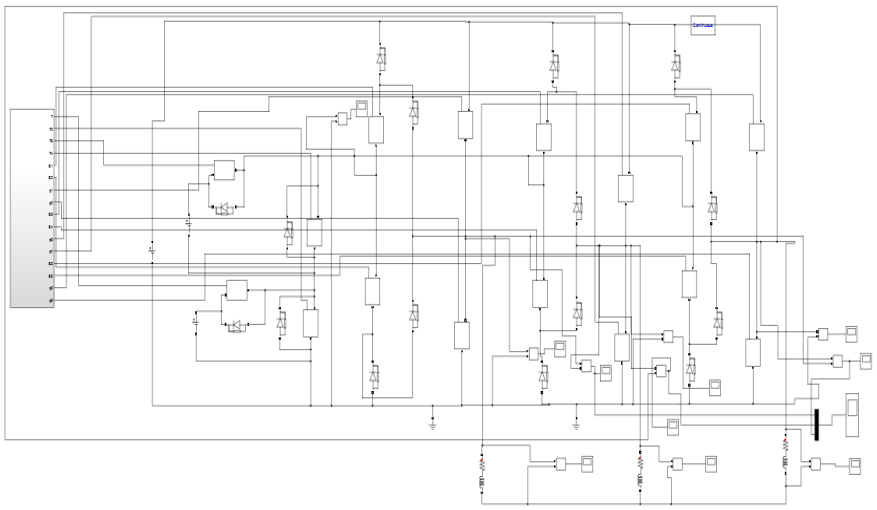

Fig.7 Simulink model of novel three phase five level inverter (configuration 1)

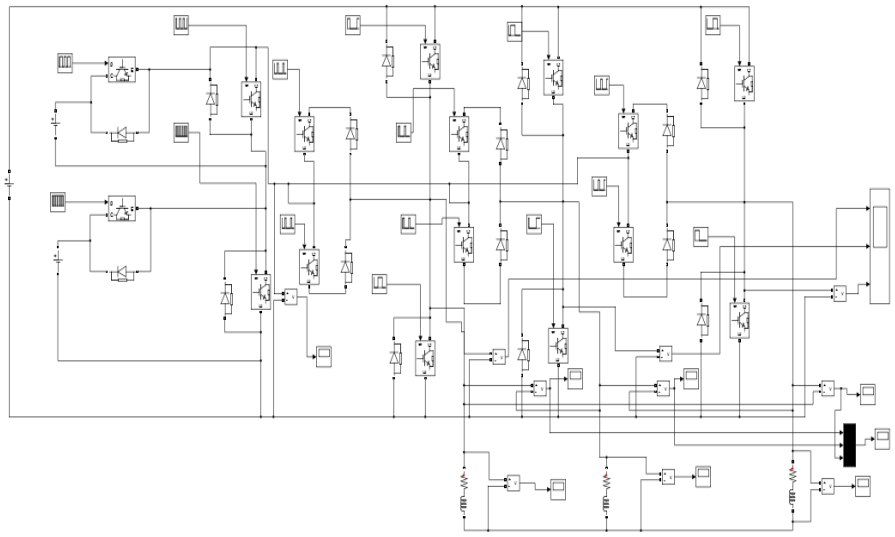

Fig.8 Simulink model of novel three phase five level inverter (configuration 2)

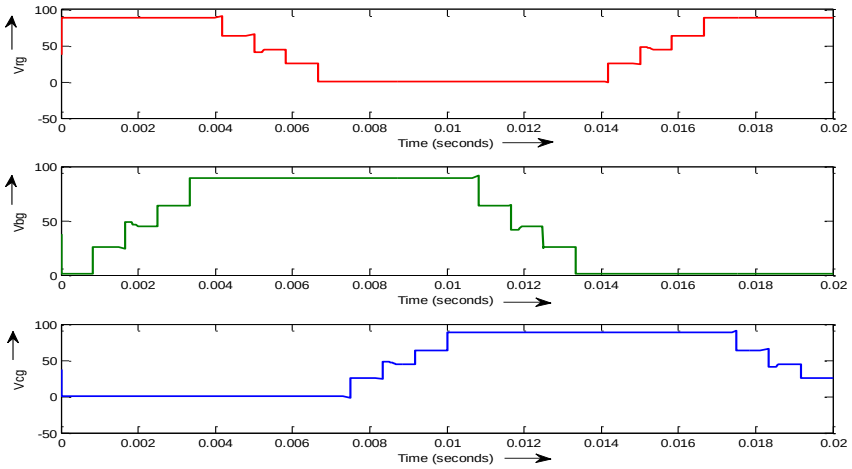

Fig.9 Simulated output waveforms of inverter line to ground voltages V_{rg},V_{yg},V_{bg}

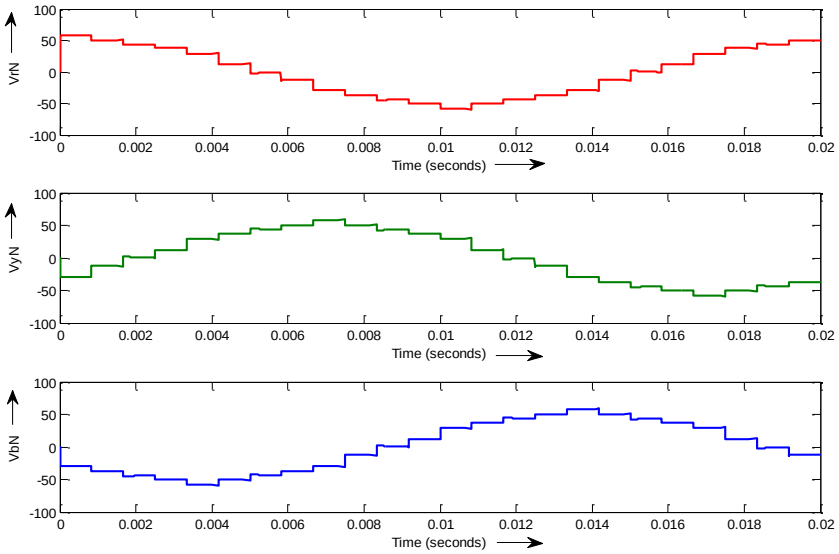

Fig.10 Simulated output waveforms of Phase voltages V_{rN} ,V_{yN} ,V_{bN}

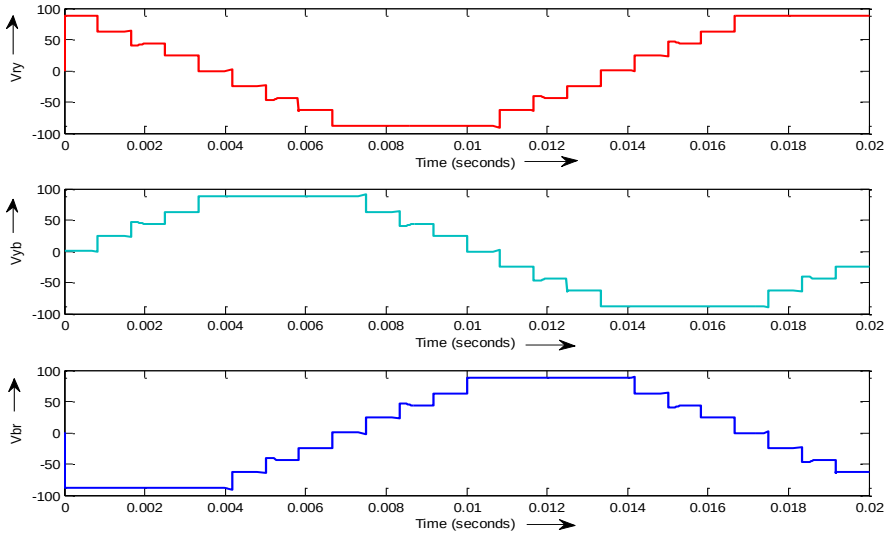

Fig.11 Simulated output waveforms of Line voltages V_{ry} ,V_{yb},V_{br}

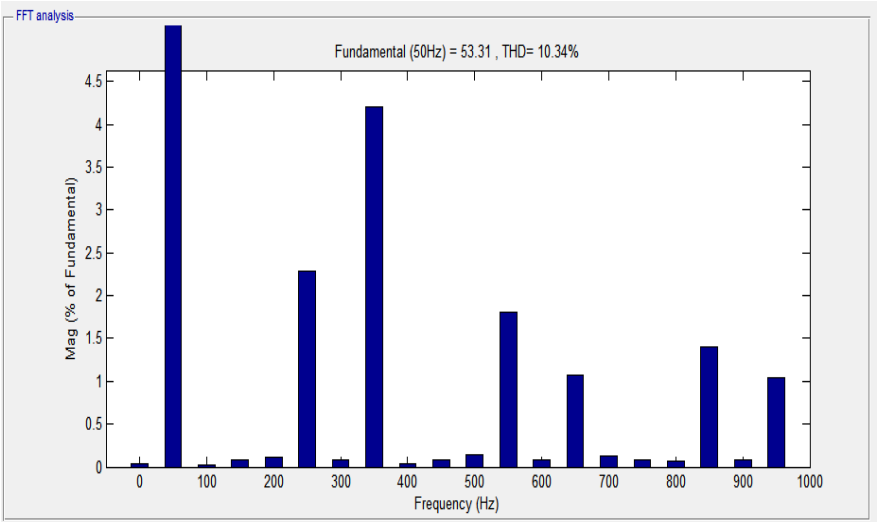

Fig.12 Total Harmonics Distortion of novel three phase five level phase voltage shows 10.34%

VII. Conclusion

The novel topology of three phase five level inverter was introduced. The proposed configuration was obtained from minimized number of power electronics elements. Therefore, the novel topology results in reduction of installation area, price and obtained lower %THD. Hence subsequent work in future may include an extension to high level with other recommended methods.

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